II. Amendments to the Claims:

This listing and version of the claims replace all prior versions, and listings, of claims in the application.

1-12. (Canceled)

13. (Previously Presented) A circuit for electrostatic discharge (ESD) protection, comprising:

an ESD protection circuit having a stack of cascaded NMOS transistors configured to discharge an ESD pulse;

a sensor that senses the ESD pulse and generates a high state voltage at an output terminal of the sensor in response to the ESD pulse; and

an inverter coupled to the output terminal of the sensor and the ESD circuit, wherein the sensor applies the high state voltage to an input terminal of the inverter.

14. (Canceled)

15. (Previously Presented) The circuit of claim 13, wherein the sensor comprises:

a voltage drop circuit coupled to the input terminal of the sensor, wherein a voltage drop occurs across the voltage drop circuit and the high state voltage is generated at the output terminal of the sensor when the input terminal of the sensor is coupled to a voltage generated by the ESD pulse; and

a device coupled to the voltage drop circuit, wherein the device is adapted to maintain the high state voltage at the output terminal, while the input terminal of the sensor is coupled to the ESD voltage pulse.

16. (Original) The circuit of claim 15, wherein the input terminal of the sensor is coupled to a voltage supply terminal.

17. (Previously Presented) The circuit of claim 15, wherein the voltage drop circuit comprises a series of diodes.

18. (Original) The circuit of claim 17, wherein the series of diodes has about 3 to about 8 diodes.

19. (Original) The circuit of claim 15, wherein the device comprises a metal-oxide-semiconductor (MOS) transistor.

20. (Original) The circuit of claim 19, wherein the MOS transistor of the device is a N-type MOS (NMOS) transistor.

21. (Original) The circuit of claim 20, wherein a gate terminal and a drain terminal of the NMOS transistor of the device are common.

22. (Canceled)

23. (Previously Presented) A method for electrostatic discharge (ESD) protection, comprising:

sensing an ESD pulse; and

pulling down an input of an ESD protection circuit to a low state voltage when the ESD pulse is sensed, wherein the ESD protection circuit comprises a stack of cascaded NMOS transistors configured to discharge the ESD pulse.

24. (Original) The method of claim 23, wherein the step of sensing the ESD pulse is performed by a sensor.

25. (Original) The method of claim 24 further comprising connecting the sensor to a voltage supply terminal to sense the ESD pulse.

26. (Original) The method of claim 25 further comprising generating a high state voltage at an output terminal of the sensor when the ESD pulse is sensed.

27. (Original) The method of claim 26 further comprising connecting the output terminal of the sensor to an inverter to generate a low state voltage at an output terminal of the inverter when the ESD pulse is sensed.

28. (Previously Presented) The method of claim 27 further comprising connecting the output terminal of the inverter to the input of the ESD protection circuit.

29. (New) A circuit for electrostatic discharge (ESD) protection, comprising:

an ESD protection circuit having a stack of cascaded NMOS transistors configured to discharge an ESD pulse;

a sensor that senses the ESD pulse and generates a high state voltage at an output terminal of the sensor in response to the ESD pulse; and

an inverter coupled to the output terminal of the sensor and the ESD circuit, wherein the sensor applies the high state voltage to an input terminal of the inverter,

wherein an input to the stack of cascaded NMOS transistors of the ESD protection circuit is pulled down to a low state voltage by an output voltage of the inverter when the sensor senses the ESD pulse.